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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,077	07/31/2003	Gerard Chauvel	TI-35638 (1962-05422)	2220
23494	7590	10/12/2007	EXAMINER	
TEXAS INSTRUMENTS INCORPORATED			TO, JENNIFER N	
P O BOX 655474, M/S 3999			ART UNIT	PAPER NUMBER
DALLAS, TX 75265			2195	
NOTIFICATION DATE		DELIVERY MODE		
10/12/2007		ELECTRONIC		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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[uspto@dlemail.itg.ti.com](mailto:uspto@dlemail.itg.ti.com)

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/632,077	CHAUVET ET AL.
	<b>Examiner</b>	<b>Art Unit</b>
	Jennifer N. To	2195

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 06 August 2007.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-26 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 31 July 2003 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>09/25/2007</u>	5) <input type="checkbox"/> Notice of Informal Patent Application
	6) <input type="checkbox"/> Other: _____

## **DETAILED ACTION**

1. Claims 1-26 are pending for examination.
2. The disclosure is objected to because of the following informalities: the newly amendments to the specification paragraph [0001] had two issues need to be resolved:
  - i. the last 3 lines from paragraph [0001] of the original specification was removed from the specification. If applicant intended to keep these last 3 lines, then applicant need to insert these 3 lines back to paragraph [0001] with an update status of the related application.
  - ii. in the newly amended specification, the newly last 3 lines of paragraph [0001] in the newly amended specification need to be removed because they are directed to "this application".

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 13-14, and 20-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Woolsey et al. (hereafter Woolsey) (U.S. Patent No. 6029000).

5. As per claim 1, Woolsey teaches the invention as claim including a system comprising:

a first processor (fig. 3, host processor 12);

a second processor (fig. 3, DSP 16) coupled to the first processor (figs. 3, 5; col. 2, lines 34-38);

an operating system configured to execute exclusively on the first processor (fig. 2, host RTOS 56 is an operating system configured to execute on host process 12; col. 3, lines 36-40); and

middle layer software configured to execute on the first processor and configured to distributed tasks to run on either or both processors (fig. 5; col. 3, lines 24-26; col. 4, lines 34-66; col. 19, lines 47-59).

6. As per claim 2, Woolsey teaches that wherein the middle layer software comprises a Java virtual machine (fig. 5, item 44).

7. As per claims 13-14, and 20-21, they are rejected for the same reason as claims 1-2 above.

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 3-5, 15, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woolsey et al. (hereafter Woolsey) (U.S. Patent No. 6029000), as applied in claim 1 above, and in view of Bolan et al. (hereafter Bolan) (U.S. Patent No. 5210828).

10. Bolan was cited in the previous office action.

11. As per claim 3, Woolsey teaches the invention substantially as claimed in claim 1. Woolsey did not specifically teach a synchronization unit coupled to the first and second processors, said synchronization unit configured to synchronize the execution of the first and second processors.

12. However, Bolan teaches a synchronization unit coupled to the first and second processors, said synchronization unit configured to synchronize the execution of the first and second processors (fig. 1, item 50, the synchronization is done using the inter-processor communications facility).

13. It would have been obvious to one of an ordinary skill in the art at the time the invention was made to have combined the teaching of Woolsey and Bolan because Bolan's teaching of a synchronization unit configured to synchronize the execution of the first and second processors would improve the integrity of Woolsey's system by

enabling the processors to communicate in a fast and efficient manner (Bolan, abstract, lines 8-9).

14. As per claim 4, Bolan teaches that the synchronization unit is configured to cause the first processor to transition to a wait mode while the second processor executes a task (col. 8, lines 64-88).

15. As per claim 5, Bolan teaches that wherein the first processor is configured to transition from the wait mode to a fully operational mode by a signal assert by either the first or second processor to the synchronization unit (col. 8, lines 64-68; col. 9, lines 30-40).

16. As per claims 15, 22, they are rejected for the same reason as claim 3 above.

17. Claims 6-12, 16-19, and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Woolsey et al. (hereafter Woolsey) (U.S. Patent No. 6029000), as applied in claim 1 above, and in view of Chauvel et al. (hereafter Chauvel) (U.S. Publication No. 2002/00624427).

18. Chauvel was cited in IDS filed 09/25/2007.

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19. As per claim 6, Woolsey teaches the invention substantially as claimed in claim 1. Woolsey did not specifically teach a shared TLB configured to contain a plurality of entries in which virtual-to-physical address translations are stored, each entry also comprising a task ID field in which a task ID associated with the corresponding translation and with a task running on the first or second processor is stored.

20. However, Chauvel teaches a shared TLB configured to contain a plurality of entries in which virtual-to-physical address translations are stored, each entry also comprising a task ID field in which a task ID associated with the corresponding translation and with a task running on the first or second processor is stored (paragraphs [0036], [0056]).

21. It would have been obvious to one of an ordinary skill in the art at the time the invention was made to have combined the teaching of Woolsey and Chauvel because Chauvel teaching of a shared TLB configured to contain a plurality of entries in which virtual-to-physical address translations are stored, each entry also comprising a task ID field in which a task ID associated with the corresponding translation and with a task running on the first or second processor is stored would improve the integrity of Woolsey's system by managing task processing that takes into account task processing times, resource capabilities and capacity, and other task processing need (Chauvel, paragraph [0010]).

22. As per claim 7, Chauvel teaches that wherein the operating system is configured to selectively flush at least one of the entries in the shared TLB based on task ID (paragraphs [0040]-[0042]).
23. As per claim 8, Chauvel teaches that wherein the middle layer software is configured to selectively flush at least one of the entries in the shared TLB based on task ID (paragraphs [0040]-[0042]).
24. As per claim 9, Woolsey teaches that wherein the middle layer software comprises a Java virtual machine (fig. 5, item 44).
25. As per claim 10, Chauvel teaches that wherein at least one of the shared TLB entries are invalidated, and those entries that are invalidated have task Ids that are associated with tasks that are running or have run on only one of the first or second processors (paragraph [0056]).
26. As per claim 11, Chauvel teaches that wherein the second processor has programmable context and is configured to autonomously switch its own context without support from the operating system executing on the first processor (paragraphs [0044]-[0045]).

27. As per claim 12, Chauvel teaches wherein the second processor includes a programmable task ID register which is configured to contain a value indicative of the task currently running on the second processor that is written by the middle layer software running on the first processor (paragraphs [0048]-[0049]).

28. As per claims 16-19, and 23-26, they are rejected for the same reason as claims 6, and 10-12 above.

#### ***Response to Arguments***

29. Applicant's arguments with respect to claims 1, 13 have been considered but are moot in view of the new ground(s) of rejection.

#### ***Conclusion***

30. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chang et al. (U.S. Patent No. 4638426), Chauvel et al. (U.S. publication No. 2002/0073282), and Hammond et al. (U.S. Patent No. 5940872) teach virtual memory address translation mechanism.

Novak et al. (U.S. Patent No. 5809522) teaches system and method for reducing cache flushing after context switching.

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31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer N. To whose telephone number is (571) 272-7212. The examiner can normally be reached on M-T 6AM- 3:30 PM, F 6AM- 2:30 PM.

32. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

33. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jennifer N. To  
Examiner  
Art Unit 2195

MENG-AI AN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100